the protocol implemented on on-chip bus 15. Logic within translation block 32 transforms requests used by the virtual socket interface protocol to equivalent bus requests for the protocol implemented on on-chip bus 15.

The third stage of the configurable architecture for interface block 19 is implemented as a queue block 33. A clocked buffer 37 receives and transmits control signals from/to translation block 32 via control lines 42 and receives and transmits data signals from/to translation block 32 via data lines 47. Clocked buffer 37 receives and transmits control signals from/to queue block 33 via control lines 52 and receives and transmits data signals from/to queue block 33 via data lines 57. Queue block 33 buffers control signals and data signals so that information from both logic block 10 and on-chip bus 15 can flow independently.

The fourth stage of the configurable architecture for interface block 19 is implemented as a driver block 34. A clocked buffer 38 receives and transmits control signals from/to queue block 33 via control lines 43 and receives and transmits data signals from/to queue block 33 via data lines 48. Clocked buffer 38 receives and transmits control signals from/to driver block 34 via control lines 53 and receives and transmits data signals from/to driver block 34 via data lines 58. Driver block 34 generates low-level electrical drive and receive specification of on-chip bus 15. Driver block 34 and on-chip bus 15 exchange control signals via control lines 44 and data signals via data lines 49.

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In the Claims:

Amend claims 1 and 7 as follows: